

HW Chap. 2

Dynamic Scheduling

Consider a system with functional unit total latencies:

Functional unit	Latency
Memory Load	5
Memory Store	2
Integer Add, Sub	1
Branch Delay	2
Double-precision Add	2
Double-precision Mult	6
Double-precision Div	13

The system has 1 functional unit of each of the above types. It stalls only as necessary to accommodate the stated latencies, and to accommodate true data dependencies. Consider the execution of the following code segment:

```
Loop:      ld      f2, 0(r1)
           divd    f8, f2, f0
           multd   f2, f6, f2
           ld      f4, 0(r2)
           addd    f4, f0, f4
           addd    f10, f8, f2
           addi    r1, r1, #8
           addi    r2, r2, #8
           sd      0(r2), f4
           sub     r20, r4, r1
           bnez    r20, Loop
```

1. How many cycles does sequential execution (one instruction at a time) take?
2. Show the parallel execution of the above code with stalls inserted as appropriate and described (e.g. 4 STALLS on ld).
3. How many cycles does 1 parallel iteration of the loop body take?
4. Indicate the presence of true data dependencies.
5. Reorder the parallel code to hide latencies and improve overall performance. Show the execution of the optimized code with stalls identified and described.
6. How many cycles does 1 optimized iteration of the loop body take?
7. What is the speedup of your optimized code over the sequential code?

Register Renaming

Suppose the hardware in a system has a set of available temporary registers labeled t0..t7. The hardware is able to substitute these temporary registers for those originally designated by the compiler. The compiler has generated the following code segment:

```
Loop:      ld      f4, 0(r1)
           multd   f2, f0, f2
           divd    f8, f4, f2
           ld      f4, 0(r2)
           addd    f6, f0, f4
           subd    f8, f8, f6
           sd      0(r2), f8
```

8. Indicate the presence of true data dependencies (RAW).
9. Indicate the presence of any WAR and/or WAW hazards.
10. Show the above code after register renaming, highlighting where any hazards have been eliminated.