HW Chap. 5

Cache Memory

1. Consider a direct-mapped cache with 64 lines and a block size of 16 bytes. What line number does byte address 1200 map to?

2. A system uses 32-bit addresses. How many *total* bits are required to implement a direct-mapped cache with 16KB of data and 4-byte blocks?

3. A cache consists of 4K blocks of 4 bytes each, and uses 32-bit addresses. Determine the number of sets and the *total* number of tag bits if the cache is:
   - direct-mapped
   - 2-way set associative
   - 4-way set-associative
   - fully associative

4. Suppose memory-access (load/store) instructions comprise 20% of the instructions in a program. Monitoring the program indicates a 2% MissRate for the Instruction cache and a 5% MissRate for the Data cache. The CPU has a CPI of 1.0 under ideal conditions, and a miss penalty of 80 cycles for any type of miss. How much faster would the processor run with a perfect cache (i.e. one that never misses)?